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ABSTRACT

A silicon carbide vertical MOSFET having low ON-resistance and high blocking voltage is provided. For this, a first deposition film (2) of low concentration silicon carbide of a first conductivity type is formed on the surface of a high concentration silicon carbide substrate (1) of a first conductivity type. Formed on the first deposition film (2) is a second deposition film (31) that comprises a high concentration gate region of a second conductivity type, with a first region removed selectively. A third deposition film (32) formed on the second deposition film, which comprises a second region that is wider than the selectively removed first region, a high concentration source region (5) of a first conductivity type and a low concentration gate region (11) of a second conductivity type. A low concentration base region (4) of a first conductivity type is formed in contact with the first deposition film (2) in the first and second regions.